***EE/CprE/SE 492 BIWEEKLY REPORT 05***

**Date:** October 26th, 2022 – November 8th, 2022

**Group number:**  Dec2022-20

**Project title:** i281 CPU Hardware Implementation

**Client &/Advisor:** Dr. Alexander Stoytchev

**Team Members/Role:**

Alex Kiefer (Hardware Team)

David Vachlon (Software Team)

Joseph De Jong (Hardware Team)

Saffron Edwards (Software Team)

 Patrick O’Brien (Hardware Team)

**Summary**

Over the last 2 weeks our team worked to finish the breadboard CPU datapath, and debug it for errors. We had several wiring issues that required debugging, but most of the current issues found were resolved. We also worked to complete the PCB designs for the CPU, and have most of the critical components finished and ready to order. We still have to wire the memory components of the CPU to the breadboards, as well as some of the critical busses for the datapath. We are working to finish up both the breadboard and PCB CPUs before the end of the semester.

**Past Week Accomplishments**

* **Alex Kiefer:**

Worked on Bus Mux PCBS and made changes to the Program Counter PCB.

* **David Vachlon:** Helped Joe wire a mux module, started setting up ribbon cables required to link individual modules, learned kicad to help with PCB design, ordered requested parts, and provided general wiring assistance.
* **Joseph De Jong:** David, Alex and Joseph worked to build three additional mux modules. These muxes were needed to compensate for design changes made throughout the planning phase. These muxes will be used during startup, user interface, and data selection.
* **Saffron Edwards:** Started compiling all progress reports, photos, and sketches into a project binder. Provided discussion and insight into Software Engineering curriculum for future of project.
* **Patrick O’Brien:** Debugged several connections along the breadboard datapath. Finished the ALU PCB, and discussed changes to be made to the switches and clock module PCBs.

**Pending Issues**

* **David Vachlon:** Need a finalized layout of the breadboard modules so that I can continue to cut and add requested ribbon cables (of appropriate length) to this implementation.
* **Alex Kiefer:**

Finish the main breadboard implementation of the CPU

* **Joseph De Jong:** Joseph needs to finish the Graphics Processor PCB design. The schematic is complete but the layout is still in progress. Alex and Patrick will check the layout and schematic after completion.
* **Patrick O’Brien:** Needs to finish the final clock/switches PCB, and get the breadboard connections to the memory modules completed.
* **Saffron Edwards:** Continue project binder and assist teammates with any components that need finishing, along with website updates before next PIRM.

**Individual Contributions**

| **NAME**  | **Individual Contributions**  | **Hours this** **week** | **HOURS** **cumulative** |
| --- | --- | --- | --- |
| Alex Kiefer | Program Counter PCB |  3 | 48 |
| David Vachlon | EEPROM wiring and module connection wiring | 3 | 50 |
| Joseph De Jong | Building breadboard datapath/ GPU | 4 | 52 |
| Saffron Edwards | Breadboard help, software discussions, and binder work | 3 | 29 |
| Patrick O’Brien |  ALU PCB, breadboard debugging and rewiring | 3 | 50 |

**Plans for the Coming Week**

* **Hardware:** Finish up the complete datapath for the breadboard CPU. Begin to debug the completed datapath and test for functionality. Finish up all necessary PCBs, and get all parts ordered.
* **Software:** Package and document the EEPROM programming software that was created for this project. Additionally, include references to the web resources used to figure out how to write it. We will also continue to update the website.

**Summary of Weekly Advisor Meeting**

The last two weeks of advisor meetings covered various issues. These include:

* There is a very short timeline to get the PCBs finished and ordered, it is necessary to get them completed as soon as possible so they can arrive before the end of the semester.

Each member discussed their concerns on the topics listed above. Eventually, a consensus was found, and design choices were implemented.